L Number	Hits	Search Text	DB	Time stamp
1	15	Test adj bus adj architecture and embed$ and RAM and operat$4	USPAT; US-PGPUB; EPO; JPO	2003/09/15 12:31
2	3729	Test and bus and architecture and embed$ and RAM and operat$4	USPAT; US-PGPUB; EPO; JPO	2003/09/15 12:31
4	233	Test$ and bus$3 and architectur$ and embed$ and RAM$2 and operat$4 and random$ and assess$ and switch$4 and control$5 and transmi$ and multiplex$ and port$2 and writ$$	USPAT; US-PGPUB; EPO; JPO	2003/09/15 12:37
5	43	Test$ and bus$3 and architectur$ and embed$ and RAM$2 and operat$4 and random$ and assess$ and switch$4 and control$5 and transmi$ and multiplex$ and port$2 and writ$$ and clock and signal$ and latch$ and command$ and pad$2	USPAT; US-PGPUB; EPO; JPO	2003/09/15 12:40
6	43	Test$ and bus$3 and architectur$ and embed$ and RAM$2 and operat$4 and random$ and assess$ and switch$4 and control$5 and transmi$ and multiplex$ and port$2 and writ$$ and clock and signal$ and latch$ and command$ and pad$2	USPAT; US-PGPUB; EPO; JPO	2003/09/15 13:00
7	728	Test$ and bus$3 and architectur$ and embed$ and RAM$2 and operat$4 and random$ and access$ and switch$4 and control$5 and transmi$ and multiplex$ and port$2 and writ$$ and clock and signal$ and latch$ and command$ and register$2	USPAT; US-PGPUB; EPO; JPO	2003/09/15 13:03
8	7	Test$ and bus$3 and architectur$ and embedded adj RAM$2 and operat$4 and random$ and access$ and switch$4 and control$5 and transmi$ and multiplex$ and port$2 and writ$$ and clock and signal$ and latch$ and command$ and register$2	USPAT; US-PGPUB; EPO; JPO	2003/09/15 13:11
9	8	Test$ and bus$3 and embedded adj RAM$2 and operat$4 and random$ and access$ and switch$4 and control$5 and transmi$ and multiplex$ and port$2 and writ$$ and clock and signal$ and latch$ and command$ and register$2 and plural$	USPAT; US-PGPUB; EPO; JPO	2003/09/15 13:12
–	10	test adj bus adj architecture and embed$ and RAM and operat$4	USPAT	2003/09/15 09:48
–	10	Test adj bus adj architecture and embed$ and RAM and operat$4	USPAT	2003/09/15 12:28

	U	1	Document ID	Issue Date	Pages	Title	Current OR
1	☒	☐	US 20030110344 A1	20030612	224	Communications systems, apparatus and methods	711/100
2	☒	☐	US 20030009712 A1	20030109	13	Test bus architecture for embedded RAM and method of operating same	714/718
3	☒	☐	US 6519104 B1	20030211	40	Computer system comprising a host connected to a disk drive employing read channel IC with common port for data and servo	360/51
4	☒	☐	US 6400715 B1	20020604	81	Network address matching circuit and method	370/392
5	☒	☐	US 6278568 B1	20010821	40	Disk drive employing read channel IC with common port for data and servo	360/51
6	☐	☒	US 5568437 A	19961022	19	Built-in self test for integrated circuits having read/write memory	365/201
7	☐	☒	US 5515540 A	19960507	32	Microprocessor with single pin for memory wipe	713/200

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1	709/200		Szczepanek, Andre et al.	☐	☐	☐	☐	☐	☐	☐	US 20030110344	☐
2			Lukanc, Jeffrey	☐	☐	☐	☐	☐	☐	☐	US 20030009712	☐
3	360/46; 360/77.08		Cloke, Robert L. et al.	☐	☐	☐	☐	☐	☐	☐	US 6519104	☐
4	370/402		Beaudoin, Denis R. et al.	☐	☐	☐	☐	☐	☐	☐	US 6400715	☐
5	360/46; 360/77.08		Cloke, Robert L. et al.	☐	☐	☐	☐	☐	☐	☐	US 6278568	☐
6	365/189.07; 714/718		Jamal, Kamran	☒	☐	☐	☐	☐	☐	☐	US 5568437	☐
7	713/194; 713/300		Grider, Stephen N. et al.	☒	☐	☐	☐	☐	☐	☐	US 5515540	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
1	☒	☐	US 20020018513 A1	20020214	99	Memory	374/178
2	☒	☐	US 20020012525 A1	20020131	253	Enhancing operations of video tape cassette players	386/69
3	☒	☐	US 6546507 B1	20030408	65	Method and apparatus for operational envelope testing of busses to identify halt limits	714/43
4	☐	☐	US 6502212 B1	20021231	65	Method and apparatus for bus parameter optimization using probes of system configurations	714/43
5	☒	☐	US 6473871 B1	20021029	64	Method and apparatus for HASS testing of busses under programmable control	714/715
6	☒	☐	US 6330977 B1	20011218	124	Electronic labeling systems and methods and electronic card systems and methods	235/487
7	☒	☐	US 6329139 B1	20011211	194	Automated sorting system for matrices with memory	435/6
8	☒	☐	US 6217234 B1	20010417	237	Apparatus and method for processing data with an arithmetic unit	709/247
9	☒	☐	US 6217213 B1	20010417	125	Temperature sensing systems and methods	374/178
10	☒	☐	US 6157621 A	20001205	143	Satellite communication system	370/310
11	☒	☐	US 6141721 A	20001031	334	Method of asynchronous memory access	711/1

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1	374/163; 374/170		Curry, Stephen M. et al.	☐	☐	☐	☐	☐	☐	☐	US 20020018513	☐
2	386/83; 386/95		Yuen, Henry C. et al.	☐	☐	☐	☐	☐	☐	☐	US 20020012525	☐
3	714/32		Coyle, Joseph P. et al.	☐	☐	☐	☐	☐	☐	☐	US 6546507	☐
4	710/15		Coyle, Joseph P. et al.	☒	☐	☐	☐	☐	☐	☐	US 6502212	☐
5	714/745		Coyle, Joseph P. et al.	☐	☐	☐	☐	☐	☐	☐	US 6473871	☐
6	235/492		Hass, Steven N. et al.	☐	☐	☐	☐	☐	☐	☐	US 6330977	☐
7	209/597; 209/604; 702/19; 702/20		Nova, Michael P. et al.	☐	☐	☐	☐	☐	☐	☐	US 6329139	☐
8			Dewar, Kevin D. et al.	☐	☐	☐	☐	☐	☐	☐	US 6217234	☐
9	368/202; 374/102		Curry, Stephen M. et al.	☐	☐	☐	☐	☐	☐	☐	US 6217213	☐
10	370/394; 370/400; 370/474		Brown, Alison K. et al.	☐	☐	☐	☐	☐	☐	☐	US 6157621	☐
11	365/189.04; 365/230.02; 365/230.06; 711/105; 711/167; 711/168		Patterson, Donald William et al.	☐	☐	☐	☐	☐	☐	☐	US 6141721	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
12	☒	☐	US 6122704 A	20000919	138	Integrated circuit for identifying an item via a serial port	711/100
13	☒	☐	US 6119213 A	20000912	234	Method for addressing data having variable data width using a fixed number of bits for address and width defining fields	711/202
14	☒	☐	US 6112275 A	20000829	111	Method of communicating over a single wire bus between a host device and a module device which measures thermal accumulation over time	711/100
15	☒	☐	US 6091884 A	20000718	243	Enhancing operations of video tape cassette players	386/83
16	☒	☐	US 6036101 A	20000314	129	Electronic labeling systems and methods and electronic card systems and methods	235/492
17	☒	☐	US 6016255 A	20000118	117	Portable data carrier mounting system	361/807
18	☒	☐	US 5995727 A	19991130	237	Video decompression	709/247
19	☒	☐	US 5984512 A	19991116	236	Method for storing video information	709/219
20	☒	☐	US 5963154 A	19991005	235	Technique for decoding variable and fixed length codes	341/67
21	☒	☐	US 5937202 A	19990810	219	High-speed, parallel, processor architecture for front-end electronics, based on a single type of ASIC, and method use thereof	712/19

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
12	711/162; 712/1		Hass, Steven N. et al.	☐	☐	☐	☐	☐	☐	☐	US 6122704	☐
13	711/203; 711/212; 711/220		Robbins, William P.	☐	☐	☐	☐	☐	☐	☐	US 6119213	☐
14	710/100; 710/107; 711/1; 711/4		Curry, Stephen M. et al.	☐	☐	☐	☐	☐	☐	☐	US 6112275	☐
15	386/46; 386/95		Yuen, Henry C. et al.	☐	☐	☐	☐	☐	☐	☐	US 6091884	☐
16	235/439; 235/441		Hass, Steven N. et al.	☐	☐	☐	☐	☐	☐	☐	US 6036101	☐
17	361/809		Bolan, Michael L. et al.	☐	☐	☐	☐	☐	☐	☐	US 6016255	☐
18			Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5995727	☐
19	345/716		Jones, Anthony Mark et al.	☐	☐	☐	☐	☐	☐	☐	US 5984512	☐
20			Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5963154	☐
21	712/11		Crosetto, Dario B.	☐	☐	☐	☐	☐	☐	☐	US 5937202	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
22	☒	☐	US 5878273 A	19990302	236	System for microprogrammable state machine in video parser disabling portion of processing stages responsive to sequence.sub.-- end token generating by token generator responsive to received data	710/5
23	☒	☐	US 5872967 A	19990216	197	Method for warm boot from reset	713/2
24	☒	☐	US 5835792 A	19981110	240	Token-based adaptive video processing arrangement	710/68
25	☒	☐	US 5829007 A	19981027	236	Technique for implementing a swing buffer in a memory array	711/5
26	☒	☐	US 5828907 A	19981027	242	Token-based adaptive video processing arrangement	710/68
27	☒	☐	US 5821885 A	19981013	236	Video decompression	341/67
28	☒	☐	US 5801973 A	19980901	236	Video decompression	708/203
29	☒	☐	US 5801958 A	19980901	95	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	716/18
30	☒	☐	US 5798719 A	19980825	240	Parallel Huffman decoder	341/67
31	☒	☐	US 5768629 A	19980616	240	Token-based adaptive video processing arrangement	710/68

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
22	712/220		Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5878273	☐
23			DeRoo, David T. et al.	☐	☐	☐	☐	☐	☐	☐	US 5872967	☐
24	345/506; 712/36		Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5835792	☐
25	345/567; 345/571; 365/189.04; 365/230.04; 365/230.05; 711/104; 711/168		Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5829007	☐
26	345/506; 712/36		Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5828907	☐
27			Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5821885	☐
28			Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5801973	☐
29			Dangelo, Carlos et al.	☐	☐	☐	☐	☐	☐	☐	US 5801958	☐
30	341/65; 704/200.1		Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5798719	☐
31	345/506; 712/36		Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5768629	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
32	☒	☐	US 5761697 A	19980602	113	Identifiable modules on a serial bus system and corresponding identification methods	711/100
33	☒	☐	US 5740460 A	19980414	241	Arrangement for processing packetized data	348/473
34	☒	☐	US 5717944 A	19980210	67	Autonomous SIMD/MIMD processor memory elements	712/20
35	☒	☐	US 5713037 A	19980127	70	Slide bus communication functions for SIMD/MIMD array processor	702/33
36	☒	☐	US 5703793 A	19971230	239	Video decompression	382/232
37	☒	☐	US 5619066 A	19970408	138	Memory for an electronic token	257/679
38	☒	☐	US 5555201 A	19960910	95	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	716/1
39	☒	☐	US 5517015 A	19960514	110	Communication module	235/492
40	☒	☐	US 5370672 A	19941206	26	Computer-controlled neurological stimulation system	607/58
41	☒	☐	US 5353243 A	19941004	991	Hardware modeling system and method of use	703/2

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
32	710/107; 710/110; 710/113; 711/1; 711/4		Curry, Stephen M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5761697	☐
33			Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5740460	☐
34	712/14		Wilkinson, Paul Amba et al.	☐	☐	☐	☐	☐	☐	☐	US 5717944	☐
35	712/14; 712/20		Wilkinson, Paul Amba et al.	☐	☐	☐	☐	☐	☐	☐	US 5713037	☐
36	708/203		Wise, Adrian P. et al.	☐	☐	☐	☐	☐	☐	☐	US 5703793	☐
37	235/492; 257/730; 257/732		Curry, Stephen M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5619066	☐
38	703/13; 716/18		Dangelo, Carlos et al.	☐	☐	☐	☐	☐	☐	☐	US 5555201	☐
39	257/678; 257/679; 257/730; 257/732		Curry, Stephen M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5517015	☐
40			Fowler, Kim R. et al.	☐	☐	☐	☐	☐	☐	☐	US 5370672	☐
41			Read, Andrew J. et al.	☐	☐	☐	☐	☐	☐	☐	US 5353243	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
42	☒	☐	US 4650926 A	19870317	47	Electrographic system and method	178/18.02
43	☒	☐	US 4600807 A	19860715	46	Electrographic apparatus	178/18.05

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
42	178/18.05; 178/20.03; 345/178		Nakamura, Shoichiro et al.	☐	☐	☐	☐	☐	☐	☐	US 4650926	☐
43	178/20.03; 345/173		Kable, Robert G.	☐	☐	☐	☐	☐	☐	☐	US 4600807	☐

L Number	Hits	Search Text	DB	Time stamp
1	10	Test adj bus adj architecture and embed$ and RAM and operat$4	USPAT	2003/09/15 09:48
2	10	test adj bus adj architecture and embed$ and RAM and operat$4	USPAT	2003/09/15 09:55
3	10	test adj bus adj architecture and embed$ and RAM and operat$4 and multiplex$	USPAT	2003/09/15 09:55
4	15	test adj bus adj architecture and embed$ and RAM and operat$4 and multiplex$	USPAT; US-PGPUB; EPO; JPO	2003/09/15 09:57

C:\APPS\EAST\Workspaces\887913.wsp

	U	1	Document ID	Issue Date	Pages	Title	Current OR
1	☐	☐	US 20030009712 A1	20030109	13	Test bus architecture for embedded RAM and method of operating same	714/718
2	☐	☐	US 20020073380 A1	20020613	89	Block based design methodology with programmable components	716/1
3	☒	☐	US 20020016952 A1	20020207	81	Block based design methodology	716/18
4	☒	☐	US 20020002691 A1	20020103	42	Method and apparatus for processor emulation	714/28
5	☒	☐	US 20010042237 A1	20011115	80	Block based design methodology	716/8
6	☒	☐	US 6594800 B2	20030715	71	Block based design methodology	716/1
7	☒	☐	US 6574778 B2	20030603	70	Block based design methodology	716/1
8	☒	☐	US 6567957 B1	20030520	71	Block based design methodology	716/4
9	☒	☐	US 6269467 B1	20010731	71	Block based design methodology	716/1
10	☒	☐	US 6189115 B1	20010213	41	Boundary scan input output serializer (BIOS) circuit	714/28
11	☒	☒	US 6006343 A	19991221	42	Method and apparatus for streamlined testing of electrical circuits	714/28
12	☒	☐	US 5687312 A	19971111	42	Method and apparatus for processor emulation	714/28
13	☒	☐	US 5677915 A	19971014	46	Customized method and apparatus for streamlined testing a particular electrical circuit	714/726
14	☒	☐	US 5606566 A	19970225	42	Method and apparatus for streamlined concurrent testing of electrical circuits	714/729

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1			Lukanc, Jeffrey	☒	☐	☐	☐	☐	☐	☐	US 20030009712	☐
2			Cooke, Laurence H. et al.	☒	☐	☐	☐	☐	☐	☐	US 20020073380	☐
3	716/2		Chang, Henry et al.	☐	☐	☐	☐	☐	☐	☐	US 20020016952	☐
4			Whetsel, Lee D.	☐	☐	☐	☐	☐	☐	☐	US 20020002691	☐
5			Chang, Henry et al.	☐	☐	☐	☐	☐	☐	☐	US 20010042237	☐
6	716/11; 716/4		Chang, Henry et al.	☐	☐	☐	☐	☐	☐	☐	US 6594800	☐
7	716/4		Chang, Henry et al.	☐	☐	☐	☐	☐	☐	☐	US 6574778	☐
8	716/1		Chang, Henry et al.	☐	☐	☐	☐	☐	☐	☐	US 6567957	☐
9	716/18		Chang, Henry et al.	☐	☐	☐	☐	☐	☐	☐	US 6269467	☐
10	714/726		Whetsel, Lee D.	☐	☐	☐	☐	☐	☐	☐	US 6189115	☐
11	714/727		Whetsel, Lee D.	☐	☐	☐	☐	☐	☐	☐	US 6006343	☐
12	703/24		Whetsel, Lee D.	☐	☐	☐	☐	☐	☐	☐	US 5687312	☐
13	702/117		Whetsel, Lee D.	☐	☐	☐	☐	☐	☐	☐	US 5677915	☐
14	702/117; 714/734		Whetsel, Lee D.	☐	☐	☐	☐	☐	☐	☐	US 5606566	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
15	☒	☒	US 5526365 A	19960611	42	Method and apparatus for streamlined testing of electrical circuits	714/726

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
15			Whetsel, Lee D.	☐	☐	☐	☐	☐	☐	☐	US 5526365	☐

09/15/2003, EAST Version: 1.04.0000